Paradigm Shift in Manufacturing Operation Through Implementation of Intelligent Dispatching

MA Chik, Ibrahim Ahmad, Mohd Yusoff Jamaludin
Department of Electrical, Electronic and System
Faculty of Engineering, University Kebangsaan Malaysia, Malaysia
azizi@eng.ukm.my; ibrahim@eng.ukm.my; myj@eng.ukm.my

ABSTRACT

Typically, wafer fabrication takes 40-60 days cycle time or more than 500 hundred processing steps that usually visited to the same tool, to complete the overall process. Thus its provides a very challenging problems in production planning and scheduling to maintain the cycle time variation between product to product because of the unique features of the wafer fabrication plant. Analyzing this issue, one of the breakdowns caused is at the queue time of the operator to make and analyze the decision to choose right lot to be dispatched. This paper will focus on the implementation of the intelligent dispatching that using commercial software to help to guide operator to select the right lot at the right time through real time lot sequencing in the FAB production floor at the respective tool. The result of the implementation has improved overall cycle time variation and bottleneck tool from 10 to 30% respectively. This project has successfully implemented in the real 200mm wafer foundry.

Keywords; Real Time Dispatch (RTD), Manufacturing Execution System (MES), Auto Simulation Family (APF), Computer Integrated Manufacturing (CIM), Overall Equipment Efficiency (OEE); Theory of Constrain (TOC) and Days Per Mask layer (DPML)

1. PROBLEM STATEMENT AND OBJECTIVE

A typical semiconductor wafer FAB contains hundreds of operation stages and its production planning becomes one of the complex systems in discrete manufacturing requirements (Mohd Azizi et. al. 2002)). Normally higher throughput, minimum cycle time, corresponded to turn ration of the WIP level and meeting on time delivery are the important performance measurement criteria in a wafer FAB and highly influenced by the dispatching rule. Theoretically, it is not difficult to pre schedule jobs for each workstation in a wafer FAB; practically it is infeasible due to dynamic change of the system. Therefore the most common approach applied in the wafer FAB in doing the shop floor control is by using the dispatching rules (Manfred Miller et. al (1999)). Due to the complexity of Wafer FAB most of them usually add confusion in the algorithm and lot prioritization. The manual activities to calculate algorithm of each lot status involved many people to discuss and usually do not get good results (Li et al. (1996)). Therefore it is not surprising that only simple common sense dispatching rules such as FIFO or EDD that associated with FAB manager experience are used in the most wafer FAB (Li et al. 1996). As today evolution technology the number of wafer processing step has
increase more than double, the complexity for manual calculation are no longer can be done efficiently.

The objective of this project is to implement a standard Intelligent Dispatch System that integrated with Theory of Constrain Principal that capable to optimize overall wafer cycle time and throughput with lowest cost. The main project goal in home grown research and analysis that includes

**Project deliverables includes**

- Cycle Time variability of +/- 0.3 DPML
- High OEE percentage in Bottleneck Tool

**Project measurements are includes**

- High Usage of the Intelligent System
- Intelligent System Compliance
- Cycle Time variability of +/- 0.3 DPML
- High utilization of OEE percentage in Bottleneck Tool

2. **RESEARCH METHODOLOGY**

The implementation of intelligent dispatching is applicable to all primary process in the wafer processing area. Key items that are required in this project include

- Overall process understanding
- Cycle data collection
- Integration of Tool Interface with RTD
- Programming logic for dispatching policies
- Reports for RTD measurements like usage, compliance rule, overall cycle time and OEE.

1.

![Figure I: RTD components and Architecture](image-url)
3. RESULT AND ANALYSIS

In order to make the system function, components such as cycle time database for required processes, Factory Works, Equipment database that consists information of maintained schedule, availability, and other factors that influence the flow of lot processes. Others that are also includes are process and tool limitation. Figure I shows summary of architecture of the Intelligence dispatching.

The data collection has completed and now in the process of putting into pieces. However a summary of results analysis can be summarized into below measurement results.

3.1 RTD Usage

![RTD Usage Graph]

**Figure 2:** RTD Usage increase across the respective time period.

As the project is launch, the usage of the data is being collected from the system log file. The usage has increased and sharpened drastically and to reach the maturity. In this project the data is calculated as when the usage of RTD per respective period has changes that ranges of +/- 5 in the systems.
3.2 RTD Compliance

![SDL Compliances](image)

*Figure 3: RTD Compliances increase accordingly across the time period*

The RTD compliance actual reaching the compliance target at every end of the target time and has improved accordingly.

3.3 Overall Equipment Efficiency

![Bottleneck OEE % Trend](image)

*Figure 4: variation trend before and after implement. Its generally explain that more WIP move to Bottleneck Tool and increase the Bottleneck tool utilization*

Collective result from all aspect shows that excellent improvement in the Overall Equipment Efficiency (OEE) cycle Time variation reduction, and on time delivery. Overall Equipment Efficiency is a key measurement that helps to determine tool performance mainly derived from WIP quantity and tool available time.
3.4 Cycle Time variation Deduction

![Cycle Time Improvement Graph]

Figure 5: TOC implementation help to reduce cycle time variation, and put in control days per mask layer.

TOC also help to reduce cycle time variation by dispatch right lot at right time. In directly its make required lot to ship on schedule and help to reduce plan to actual shipment variation.

4. CONCLUSION

The challenge in this project is to collect and verify the cycle time of each individual product where intensive and long hours of data verification is being done automatically by writing up logic to collect data using commercial software that integrated with tool and also manual comparison and verification. This project is being implemented smoothly and has gets well supported from top management for manufacturing to used and executed FAB wide. In overall, as the usage and the RTD compliance has reach its pinnacle, the lot cycle time and on time delivery makes the gap for the variability smaller. The results shows an improvement of 10-25% of the lot cycle time variation and average of 20% improvement of the bottleneck tools. Others aspects in the sidelines such as reduce number of communication and better lot dispatching also get the high light from the users. In short, it concludes that the implementation of intelligent dispatching project currently show positive results and successfully been implemented in the wafer foundry.

5. REFERENCES

Mohd Azizi Chik, Yeo Eng Teck and Lim Kian Wee, 2002“ SilTerra Dispatching Systems Through Theory of Constraint” ICSE 2002, Penang Malaysia pp 43-45,
